

Press Release

SiliconPipe Technology Makes 40Gbps Copper-Backplane A Reality

SAN JOSE, Calif., November 11, 2003—SiliconPipe, Inc., has announced that it has successfully demonstrated its CleanChannel™ technology at rates of 40Gbps. The system delivered a clean signal across a backplane over 30 inches, including two interconnects, at a projected lower cost than today's 3Gbps backplane technology.

All high-speed backplanes built today are limited in bandwidth by the materials and design of the systems interconnects. At high frequencies, attenuation and reflections degrade the signal. These discontinuities in the signal path limit transmission of high frequencies and increase rise times. This rise-time degradation causes intersymbol interference (ISI), deterministic jitter and collapse of the eye diagram.

To minimize the effect of these fundamental limitations, the attenuation and reflections must be controlled. Current suppliers attempt to control these losses by using low-loss laminates, via stub back-drilling and active signal-conditioning techniques. However, these complications increase the cost of the backplane and the line cards.

SiliconPipe changing the paradigm for backplane systems

"We need to rethink what we mean by backplanes," said Thomas Obenhuber, vice president of marketing with SiliconPipe. "It is the mind set of how we build backplane systems that limits the bandwidth and upgradability. Imagine using CleanChannel Technology for 10Gbps SerDes with a power requirement of less than 100mW. Or building a 10-inch connection schema with just a simple CML driver and clock and data."

To achieve a system solution using copper media, not only is the dielectric of the material crucial but so is the performance of the interconnections. Uniform impedance must be maintained from the line-card silicon, through the line card's connector, the high-density backplane, the switch-card connector and, finally through to the switch-card silicon.

The ChannelPlane system consists of two major components: a conventional FR4 backplane containing power, ground and low-frequency signals plus an integrated second part, the Omnibus system, which carries all high-speed links over high-performance cables. The ChannelPlane system can be expanded to become a uniform connection from Integrated circuit (IC) packages on one line card, through the backplane, to IC packages on another line card, providing optimal system-level performance. Package connections that eliminate discontinuities in line cards are made close to the silicon die, using uniform low-loss interconnects. Discontinuities from vias, multilayer printed-circuit board (PCB) traces and IC substrates are eliminated. Industry-standard high-performance connectors can be used, depending on performance requirements, between the backplane and the line cards.

"Our ChannelPlane system eliminates the need to consider optical backplanes for OC-768 systems for distances up to 40 inches," said Para Segaram, founder of SiliconPipe. "Additionally, our system enables

silicon suppliers to use standard low-power 0.07-micron complementary metal-oxide semiconductor (CMOS) silicon to drive backplane channels. Transceiver vendors can provide low-power, high-performance CMOS solutions without the need for receive equalization, multilevel PAM signaling or multitap preemphasis. Conventional backplane solutions demand higher-level voltage swings, eliminating the ability to use smaller-geometry CMOS.”

“Manufacturing costs are similar to conventional high-density backplanes. This means 40Gbps performance at the cost of 3Gbps,” said Bill Wiedemann, president and CEO of SiliconPipe. “Today’s 3Gbps systems can be upgraded with new line cards as the market demands higher performance.”

SiliconPipe has patented the key technologies in the ChannelPlane system and is currently sampling.

About SiliconPipe

SiliconPipe, founded in 2002 in San Jose, California, designs and integrates complete high-performance system-interconnect solutions. SiliconPipe’s suite of novel patent-pending technologies includes IC packaging solutions; low-skew parallel line interconnects for memories, AirCore™ cable, high-speed transceivers and high-performance copper backplanes. The technologies represent significant and necessary departures from traditional concepts to cost-effectively meet the performance requirements of next-generation high-speed products. SiliconPipe has developed more than 35 patents.

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