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New Stairstep Approach Simplifies Substrate Design

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Semiconductor packaging has always been about keeping things as simple and inexpensive as possible. While a range of options now exist for low-I/O chips, intermediate and high-performance chips use essentially the same multilayer BGA substrate technology. [Silicon Pipe](#) (San Jose) has proposed a stairstep substrate specifically for wire-bonded BGAs that avoids the use of interlayer connections.



Stairstep substrates have been used in wire-bonded BGA applications before as a way to increase the wire-bond density. Because the layers are not interconnected in this substrate, each layer is connected to the board with its own set of bumps ([Fig. 1](#)).

This, of course, requires different bump sizes for the same package. Though using different bump sizes adds a complication to the design, it is a part of a scheme that simplifies everything else. Since there are no interlayer connections, there are no blind vias to line up, no vias of any kind to fill, and no need to make multiple electrical connections every time a layer is added. Each layer is made by patterning metal traces on them, and the layers are simply "glued" onto each other.

This is in contrast to a typical BGA substrate, where the one simple aspect is that the bumps are the same size. When a signal travels between the chip and the board in a typical BGA substrate, it experiences impedance changes every time it goes in or out of a via. When a high-current signal travels in or out of a via, it can produce some electromagnetic interference (EMI), and current crowding effects at the ends of a via might lead to electromigration.

A typical BGA substrate is considered to be a "controlled environment" for all the signals traveling between the chip and the board. BGA packages are proven, and the concerns mentioned above have all been addressed. However, the via-less approach can provide a simpler environment for the signals, and it reduces the manufacturing and reliability concerns to those of attaching the package to the board.



1. In this stairstep substrate design, each layer connects to the board directly.

Though board attach might be a little more challenging with this new package, it could be argued that the overall complexity is reduced, compared with a typical multilayer BGA. There are other advantages to using this new approach, all based on the concept of matching signals and mechanical requirements with the appropriate substrate characteristics.

Faster signals can be routed to I/Os that are closer to the chip. Since the smaller bumps can be placed on a tighter pitch, the I/O density can be higher for those signals. This helps in situations where high-speed signals are

routed on differential pairs.

Slower signals, power connections and high-current signals can be routed through the larger bumps at the periphery. The larger bumps can handle high-current signals better, and the timing of slower signals is less sensitive to the distance of the package I/O from the chip. Also, larger bumps can handle more lateral strain, and they are placed on the periphery where the lateral strains are larger.

Another potential advantage is analogous to one of the key advantages of systems-in-package (SiPs). Signals that absolutely require special substrate materials can have them, with less impact on the packaging cost. For example, if some signals need to be placed on ceramic materials, then those signals can be placed on one ceramic layer in a stack containing mostly organic layers, rather than using ceramic materials for the whole substrate.

There is also an advantage with regard to electrical testing. The final substrate does not really need to be tested before wire bonding. Visual inspection of each substrate layer prior to assembly might actually be sufficient ([Fig. 2](#)).

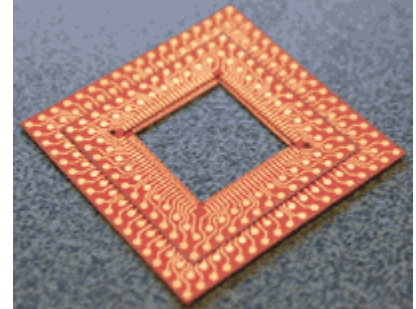
The capabilities of this package match the needs of a wire-bonded chip, and the things it cannot do are things that a wire-bonded die likely does not need. For example, it is not well suited for the use of package intermediated interconnects, but the chips that might need them are usually not wire-bonded. Conversely, if a chip's performance level is intermediate, it will not need all the capabilities of a package made for high-performance chips. The via-less package is an option that promises lower cost.

This via-less approach is a return to keeping things simple and keeping costs down by giving the signals what they need — simple paths with fewer discontinuities. It also reveals a rising theme in packaging technology. As systems become more complex, matching the characteristics of a package to the needs of the chip and its signals will become increasingly important, because that approach promises to increase efficiency and reduce expense.

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2. This package only requires simple traces on each layer, which are easy to make and test. (Source: Silicon Pipe)