

Novias™ StairStep Package Backgrounder

Novias™ StairStep BGA IC packages (Novias-SSP) provide a high-performance, low-cost substrate solution using tiered or “StairStepped” contacts at package edges which sequentially expose for interconnection layers of redistributed circuit connections with no vias or stubs. These simple no-via IC package structures provide significant performance and reliability gains while reducing manufacturing costs.

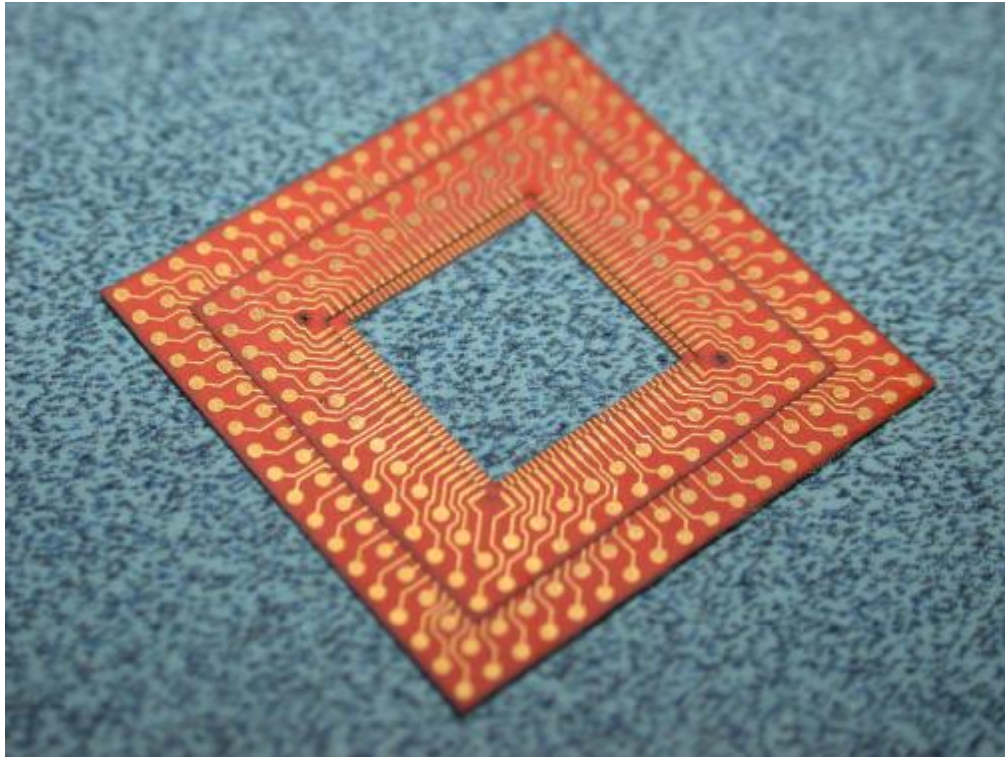


Figure 1. Novias StairStep package

Applications:

- Flexible, high performance, low cost, controlled impedance packaging
- >200 pins
- IC solutions requiring impedance control on maximum number of pins
- Multi-layer; flex or rigid
- Wirebond or flip-chip
- Microstrip and stripline
- Uni-pitch or multi-pitch
- Single or multiple die
- Custom or COTs
- Component in high-speed (>10Gbps) system when used with other SuperCharged Copper OTT or Novias components.

Materials:

- Rigid substrates (e.g., FR4, BT resin)
- Flexible substrates (e.g. Polyimide, LCP)

Packaging:

- Single die or multiple die, cavity down
- Wire bond or Flip Chip (Flip chip requires NDA)
- Heat spreader / Stiffener options

Benefits:

- Cost
 - Less material – Greater than 30% in material cost savings
 - § Each successive layer uses less material
 - Simple manufacturing techniques, fewer steps (no drilling, no plating.)
 - § Saves 100% of costs associated with via processing
 - Design costs – Signal layers are directly converted to micro-strip or strip-line through added metalization
 - § Little need for signal integrity tools/experts since vias are eliminated
- Performance
 - Via related impedance eliminated – 0% impedance change
 - Via related cross-talk eliminated – 0% via crosstalk
 - Skew is easier to manage between signals
 - Lower inductance on power feed paths
- Manufacturing
 - Uses current materials and manufacturing techniques (flex or rigid)
 - Optical inspection for electrical performance--no test probes
 - An all-lithographic process—no serial drilling
 - Continuous (reel-to-reel) flow manufacturing possible (flex)
 - Can be used for both custom (design on demand) and COTS (assemble on demand from stored layers of standard configurations)
- Reliability
 - Via defect rate eliminated – 0 ppm

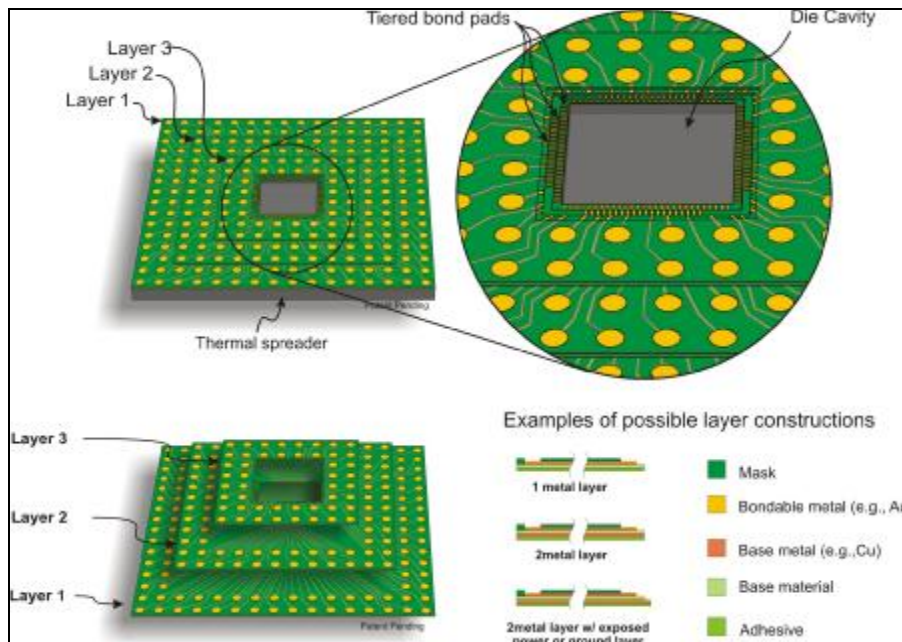


Figure 2. StairStep Package Structure for Wire Bond IC

Figure 2 illustrates a Stair Step package for wire bond ICs. The main body of the package is comprised of sequential layers of metal circuit patterns on a series of dielectric base materials that are bonded to a laminate or metal carrier base. Each sequential layer has reduced outer and slightly enlarged internal dimensions to expose both IC and substrate terminations without using plated vias. One or more IC die(s) are attached in the central cavity of the package and then wire bonded to the various tiered circuit layers. The result is a very simple and reliable, low-cost structure that is fabricated using proven and tested package assembly technology. The Novias-SSP connects to a PCB via solder balls.

Novias-SSP IC packaging is applicable to both lead frame and rigid and flexible laminate interconnection structures and can be used for both peripherally leaded and area array contact designs. With laminate interconnection structures, integral ground and power, and differential pair options, a wide range of new opportunities for high-performance in an electronically quiet environment are achievable.

Novias-SSP substrates can be quickly customized to meet both vendor and customer needs. Standardized pin count layers can be manufactured in advance and assembled to order. Because there are no holes to plate and drill, layers of redistribution circuits can be assembled to quickly meet design needs. Creating mixed pitch structures is simplified; each layer can use a different pitch (see Figure 6.) Novias-SSP IC packages can be built in a variety of shapes and sizes. I/O pitches can range from 1.50 mm to 0.50 mm; reduced pitches are available.

Not shown but available for disclosure is SiliconPipe's flip chip (solder bump) Stair-Step Package substrates. Wire bonds are entirely eliminated while maintaining consistent impedance connections from the IC to the stair step layers.

Structural Differences:

The Novias-SSP provides the advantages of a single layer substrate but eliminates signal density issues. Figure 3 summarizes the differences in structures between legacy BGA packaging and the StairStep Package.

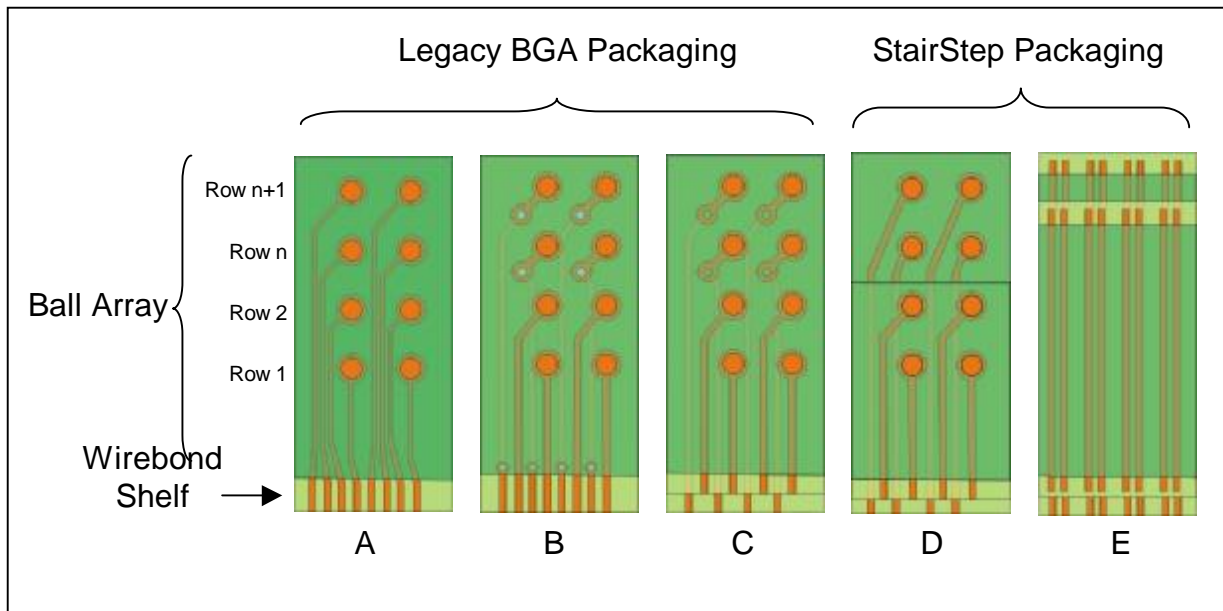


Figure 3. Signal Routing Difference

Illustration “A” shows a single layer BGA layout for signal distribution away from wire bond pads. The signal trace widths and spacing govern how many rows can be allocated for balls in a single layer. Impedance and cross-talk complicate signal trace design as frequency increases. To meet cross-talk, impedance and other important design criteria, structures like the one shown in illustration “B” are utilized. Designers may add an extra signal layer (in this case on the backside) to spread signals and relax spacing requirements. This approach requires the use of plated through-holes (vias), which become a significant source of signal interference (e.g., cross talk) as the frequency increases. The use of vias can be reduced by constructing substrates with an additional substrate layer as shown in illustration “C”. This solution halves the number of vias but adds the cost of an additional substrate layer. The natural next step in achieving a desired substrate design, total elimination of vias, is shown in illustration “D.” This approach has three major advantages:

- Elimination of vias means substrate manufacturers can dispense with drilling and plating, a major cost savings.
- Elimination of vias removes a major contributor to substrate reliability.
- Elimination of vias gives designers an opportunity to improve the signal integrity of the substrate.

Microstrip, Stripline and Power Supply Signal Benefits

Superior signal transmission characteristics are achievable with the Novias-SSP. Figure 4 shows an example of an SSP substrate capable of zero-skew and minimal cross-talk utilizing microstrip or stripline differential pairs.

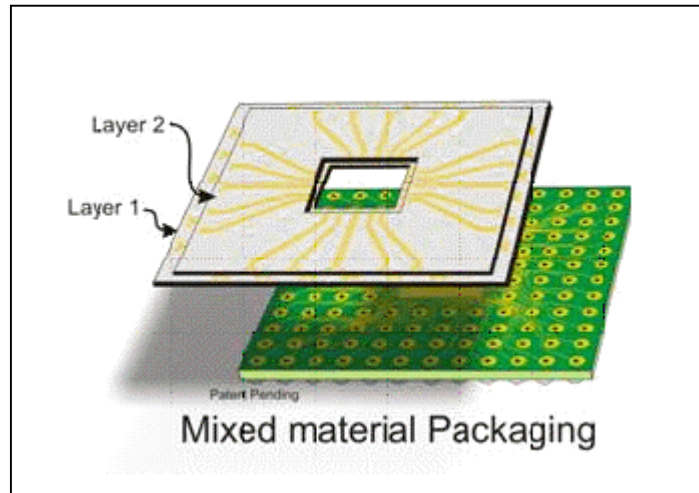


Figure 4. High Speed Layer Construction

Each stair step layer may be fabricated with a signal layer on one side and a ground or power layer on the other thus forming the needed impedance control plane(s) for either microstrip or stripline. These ground or power planes provide further benefit as power supply feeds with minimal inductance. Alternatively, power or ground feeds can co-exist interstitially among the signal pairs on each layer. In either case power supply inductance is reduced by the elimination of vias.

Usable Today and Future Proof:

Incorporating the Novias-SSP in today's designs is straightforward and does not require manufacturing or process flow changes. The thin stair stepped layers can interface to a planar PCB surface using uni-pitch solder balls which adjust via columnarization (the elongation of the outer solder balls).



Figure 5. StairStep Package Cross-Section

Alternatively, to maintain a planar contact point across all solder balls, a multi-diameter solder ball implementation is shown in Figure 6.

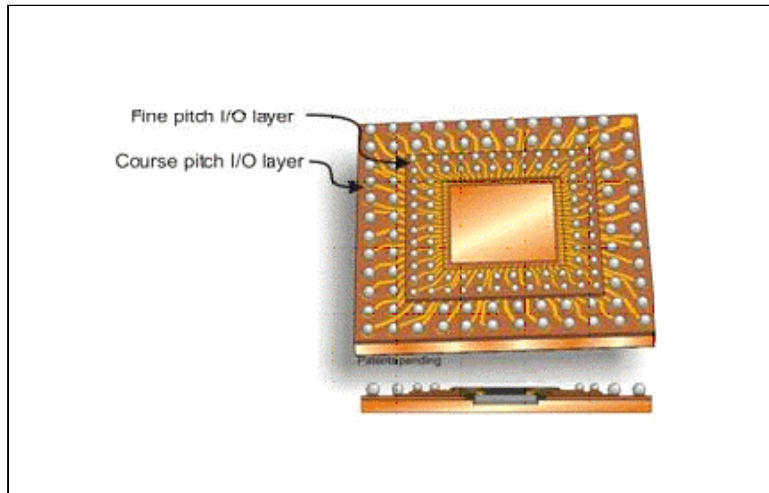


Figure 6. StairStep Package with Height Adjusted Solder Balls

A third method for maintaining contact co-planarity is illustrated in Figure 7.

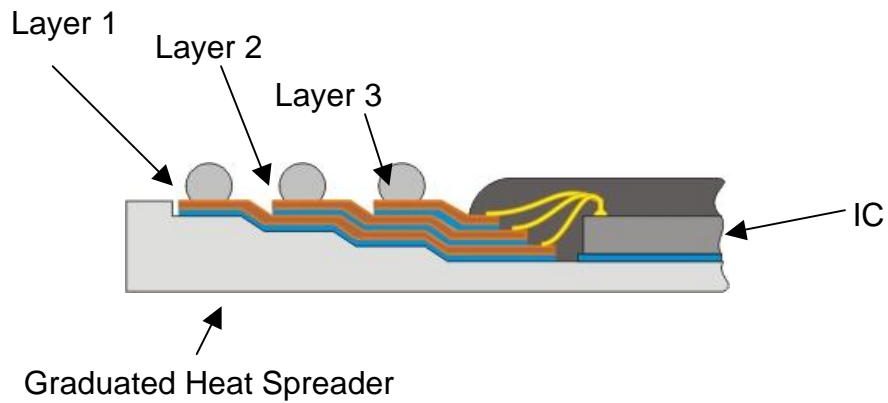


Figure 7. StairStep Package with Graduated Heat Spreader

Solder ball height is maintained by a contoured heat spreader base.

Figure 8 illustrates different methods for maintaining connection planarity:

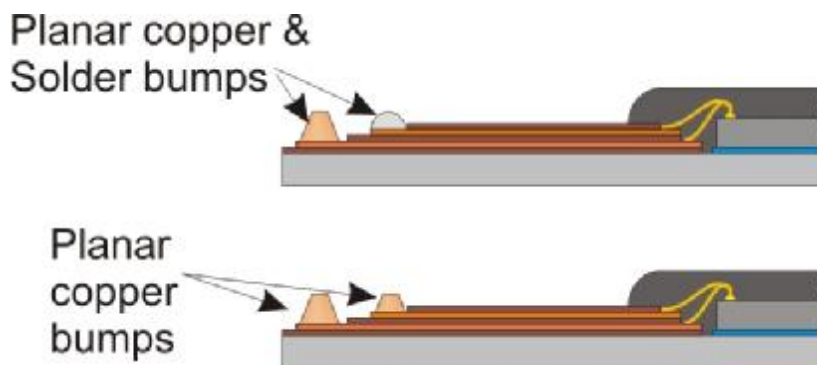


Figure 8. Alternative planarity solutions

Figure 9 shows how the StairStep Package can be combined with other SiliconPipe structures. In this example two StairStep packaged ICs are connected together via a PCB with a dedicated HS top layer that contains no vias. The HS outputs from the packages connect to the HS PCB traces using a SiliconPipe connector. LS, power and ground connections interface to the lower layers of the PCB using solder bumps.

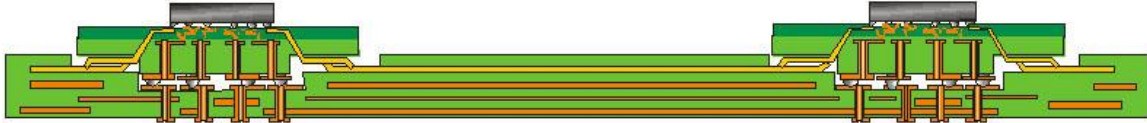


Figure 9: StairStep-based interconnect system example using two ICs with StairStep packaging that uses special SiliconPipe high-speed connections, StairStep sockets on the PCB and a Novias high-speed signaling layer on the PCB for channels linking the two ICs.